1. (Thrice Amended) A method for manufacturing an interconnect structure comprising:

forming a recess within a dielectric material situated on a semiconductor lower substrate, said recess extending below a top surface of said dielectric material;

forming a diffusion barrier layer on the recess within the dielectric material;

forming a seed layer on the diffusion barrier layer, the diffusion barrier layer being composed of a material having a melting point greater than or equal to that of a material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed;

forming an energy absorbing layer on said electrically conductive layer, said energy absorbing layer having a greater thermal absorption capacity than that of said electrically conductive layer;

applying, omnidirectionally, energy to said energy absorbing layer to cause said electrically conductive layer to flow within said recess; and

removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

2. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein forming a diffusion barrier layer on the recess within the dielectric material is a CVD deposition step.

3. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of ceramics, metallics, and intermetallics.

4. (Unchanged) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

5. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, further comprising, prior to forming a seed layer on the diffusion barrier layer, heating the diffusion barrier layer is an environment substantially containing a nitrogen gas.

6. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein depositing a seed layer on the diffusion barrier layer is a CVD deposition step.

7. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the seed layer is composed is selected from the group consisting of ceramics, metallics, and intermetallics.

8. (Unchanged) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

9. (Unchanged) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper.

10. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the energy absorbing layer is composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

11. (Twice Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein applying energy to said energy absorbing layer utilizes.

12. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein removing portions of the energy absorbing layer and the electrically conductive layer is an abrasive planarization step.

13. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 12, wherein removing portions of the energy absorbing layer and the electrically conductive layer is a chemical mechanical planarizing step.

14. (Unchanged) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the recess has an aspect ratio greater than about four (4) to one (1).

15. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the recess comprises a contact hole situated below a trench, said semiconductor substrate assembly having a lower substrate defining a plane, said contact hole terminating at an end thereof at said lower substrate and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending parallel to the plane of the lower substrate.

16. (Thrice Amended) A method for manufacturing an interconnect structure comprising:

patterning and etching a dielectric material situated on a semiconductor substrate assembly so as to form a recess within the dielectric material, said recess being situated below a top surface of said dielectric material;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of the material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer:

having a greater thermal absorption capacity than that of said electrically conductive layer; and

being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed;

heating, omnidirectionally, the energy absorbing layer to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

17. (Unchanged) A method for manufacturing an interconnect structure as recited in Claim 16, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

18. (Unchanged) A method for manufacturing an interconnect structure as recited in Claim 16, wherein the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

19. (Unchanged) A method for manufacturing an interconnect structure as recited in Claim 16, wherein the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper.

20. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 16, wherein the energy absorbing layer is composed of a material selected from the

group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

21. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 16, wherein the heating, omnidirectionally, the energy absorbing layer is performed with a furnace.

22. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 16, wherein the recess comprises a contact hole situated below a trench, said semiconductor substrate assembly having a lower substrate defining a plane, said contact hole terminating at an end thereof at said lower substrate and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending parallel to the plane of the lower substrate.

23. (Thrice Amended) A method for manufacturing an interconnect structure comprising:

patterning and etching a dielectric material situated on a semiconductor substrate assembly so as to form a recess within the dielectric material, said recess being situated below a top surface of said dielectric material;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed, the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer:

having a greater thermal absorption capacity than that of said electrically conductive layer; and

being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed,

being is composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon;

heating with a furnace the energy absorbing layer to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

24. (Thrice Amended) A method for manufacturing an interconnect structure comprising:

forming a dielectric material on a monocrystalline silicon layer of a semiconductor substrate assembly, said monocrystalline silicon layer defining a plane;

patterning and etching the dielectric material so as to form a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench being parallel to the plane of the monocrystalline silicon layer;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing a layer composed of aluminum on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of aluminum, the material from which the seed layer is composed having a melting point greater than or equal to that of aluminum;

depositing an energy absorbing layer on said layer composed of aluminum, said energy absorbing layer:

having a greater thermal absorption capacity than that of said layer composed of aluminum; and

being composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the layer composed of aluminum;

heating omnidirectionally with a furnace the energy absorbing layer to cause said layer composed of aluminum to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the layer composed of aluminum that are situated above the top surface of the dielectric material.

25. (Unchanged) A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

26. (Unchanged) A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

27. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the energy absorbing layer is composed is selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

28. (Thrice Amended) A method for manufacturing an interconnect structure comprising:

forming at least one silicon layer on a monocrystalline silicon layer of a semiconductor substrate assembly, said silicon layer being selected from the group consisting of undoped silicon dioxide, doped silicon dioxide, undoped silicate glass, and doped silicate glass, wherein said monocrystalline silicon layer defines a plane;

patterning and etching the at least one silicon dioxide layer so as to form a recess therein, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the at least one silicon layer and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said at least one silicon layer, the trench being parallel to the plane of the monocrystalline silicon layer;

depositing a diffusion barrier layer within the recess within the at least one silicon layer, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing a layer composed of aluminum on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is

composed having a melting point greater than that of aluminum, the material from which the seed layer is composed having a melting point greater than or equal to that of aluminum;

depositing an energy absorbing layer on said layer composed of aluminum, said energy absorbing layer having a greater thermal absorption capacity than that of said layer composed of aluminum and being composed of a material:

having both a higher thermal insulation capacity and electric insulation capacity than aluminum; and

selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon;

heating omnidirectionally with a furnace the energy absorbing layer to cause said layer composed of aluminum to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the layer composed of aluminum that are situated above the top surface of the at least one silicon layer.

36. (Twice Amended) A method for manufacturing an interconnect structure that includes a recess extending below a top surface of a dielectric material situated on a semiconductor substrate, the recess having therein a diffusion barrier layer that is within the dielectric material, the method comprising:

forming a seed layer on the diffusion barrier layer;

forming an electrically conductive layer on the seed layer including the portion of the seed layer within said recess;

forming upon the electrically conductive layer an energy absorbing layer having a greater thermal absorption capacity than that of the electrically conductive layer;

flowing the electrically conductive layer within the recess by omnidirectionally heating the energy absorbing layer.

37. (Once Amended) The method as defined in Claim 36, wherein the melting point of:

the diffusion barrier layer is not less than that of the seed layer and is greater than that of the electrically conductive layer; and

the seed layer is not less than that of the electrically conductive layer.

38. (Unchanged) The method as defined in Claim 36, further comprising:

removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

39. (Unchanged) The method as defined in Claim 36, wherein:

the electrically conductive layer is composed of aluminum; and

the energy absorbing layer is composed of a material selected from the group consisting of titanium nitride, tungsten, and a dielectric substance.

40. (Unchanged) The method as defined in Claim 36, wherein:

the electrically conductive layer is composed of copper; and

the energy absorbing layer is composed of a material selected from a group consisting of tungsten, titanium nitride, tantalum, and carbon.

41. (Unchanged) The method as defined in Claim 36, wherein:

the diffusion barrier layer is composed of a material selected from a group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

the seed layer is composed of a material selected from a group consisting of aluminum, titanium nitride, titanium, and titanium aluminide;

the electrically conductive layer is composed of a material selected from a group consisting of aluminum and copper; and

the energy absorbing layer is composed of a material selected from a group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

42. (Unchanged) The method as defined in Claim 36, wherein:

the diffusion barrier layer is composed of a material selected from a group consisting of aluminum nitride, tungsten nitride, and tantalum nitride;

the seed layer is composed of a material selected from a group consisting of aluminum, titanium, and titanium aluminide;

the electrically conductive layer is composed of a material selected from a group consisting of aluminum and copper; and

the energy absorbing layer is composed of a material selected from a group consisting of tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

43. (Once Amended) The method as defined in Claim 36, wherein flowing the electrically conductive layer within the recess by omnidirectionally heating the energy absorbing layer is performed with a furnace.

44. (Unchanged) The method as defined in Claim 36, wherein the seed layer comprises multiple layers, each layer in said multiple layers being composed of a material selected from the group consisting of silicon and titanium nitride.

45. (Twice Amended) A method for manufacturing an interconnect structure that includes a recess extending below a top surface of a dielectric material situated on a semiconductor substrate, the recess having therein a diffusion barrier layer that is within the dielectric material, the method comprising:

forming a seed layer on the diffusion barrier layer;

forming a first layer on the seed layer including the portion of the seed layer within said recess;

forming upon the first layer a second layer that can absorb more heat than the first layer;

heating, omnidirectionally, the first and second layers to flow the first layer within the recess by heat.

46. (Once Amended) A method for manufacturing an interconnect structure, the method comprising:

forming a dielectric material over a semiconductor substrate and having a top surface;

forming a recess within the dielectric material extending from the top surface of the dielectric material to the semiconductor substrate;

filling the recess with an electrically conductive material, the recess including:

a first portion having a uniform width and extending within the dielectric material to the top surface of the dielectric material;

a second portion having a height and a uniform width that is less than the width of the first portion and that is not greater then 25% of the height, the second portion extending from the semiconductor substrate to terminate at the first portion;

wherein the filling the recess is performed by causing the electrically conductive material to flow within the recess by applying omnidirectional heating.

47. (Unchanged) The method as defined in Claim 46, wherein the first portion is a trench having a bottom surface that extends longitudinally parallel to the top surface of the dielectric material, and the second portion is a contact plug.

48. (Twice Amended) The method as defined in Claim 46, wherein filling the recess with the electrically conductive material further comprises:

forming a diffusion barrier layer in contact with the semiconductor substrate and the dielectric material;

forming a seed layer upon the diffusion barrier layer and composed of a material having a melting point less than that of the material from which the diffusion barrier layer is composed and being selected from a group consisting of ceramics, metallics, and intermetallics;

forming a conductor layer upon the seed layer including the portion of the seed layer within said recess; and

forming an energy absorbing layer on the conductor layer that is composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the material from which the conductor layer is composed;

wherein the omnidirectional heating is performed with a furnace.

49. (Unchanged) The method as defined in Claim 48, wherein the diffusion barrier layer is upon the top surface of the dielectric material.

50. (Unchanged) The method as defined in Claim 48, wherein the diffusion barrier layer is composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

51. (Unchanged) The method as defined in Claim 48, wherein the seed layer is composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

52. (Unchanged) The method as defined in Claim 48, wherein the conductor layer is composed of a material selected from the group consisting of aluminum and copper.

53. (Unchanged) The method as defined in Claim 48, wherein the material from which the energy absorbing layer is composed is selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

54. (Once Amended) A method for manufacturing an interconnect structure, the method comprising:

forming a lower substrate situated on a semiconductor substrate assembly, said lower substrate defining a plane;

forming a dielectric material on the lower substrate having a planar top surface;

forming a recess within said dielectric material, said recess including a contact hole situated below a trench, said contact hole terminating at an end thereof at the lower substrate and terminating at an opposite end thereof at said trench, said contact hole being oriented substantially perpendicular to the plane of said lower substrate, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending substantially parallel to the plane of said lower substrate; and

forming an electrically conductive layer situated within and filling both the contact hole and the trench and extending to terminate above the planar top surface of the dielectric material;

wherein the filling both the contact hole and the trench is performed by causing the electrically conductive layer to flow into the contact hole and the trench by applying omnidirectional heating.

55. (Once Amended) The method as defined in Claim 54, wherein forming an electrically conductive layer further comprises:

forming a diffusion barrier layer in contact with the lower substrate and the dielectric material;

forming a seed layer upon the diffusion barrier layer and composed of a material having a melting point less than that of the material from which the diffusion barrier layer is composed and being selected from a group consisting of ceramics, metallics, and intermetallics;

forming a conductor layer upon the seed layer; and

forming an energy absorbing layer on the conductor layer that is composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the material from which the conductor layer is composed;

wherein the omnidirectional heating is performed with a furnace.

56. (Unchanged) The method as defined in Claim 55, wherein the contact hole has a height and a width, and the height is greater than four times the width.

57. (Twice Amended) A method for manufacturing an interconnect structure, the method comprising:

forming a lower substrate situated on a semiconductor substrate assembly, said lower substrate defining a plane;

forming a dielectric material on the lower substrate having a planar top surface;

forming a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said contact hole being oriented substantially perpendicular to the plane of said lower substrate, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending substantially parallel to the plane said lower substrate;

forming a diffusion barrier layer on the trench and the contact hole;

forming a seed layer on the diffusion barrier layer, the diffusion barrier layer being composed of a material having a melting point greater than or equal to that of a material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer within the trench and contact hole and extending to terminate at the planar top surface of the dielectric material, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed; and

applying, omnidirectionally, energy to the electrically conductive layer to cause the electrically conductive layer to flow within the recess.

58. (Unchanged) The method as defined in Claim 57, wherein the material from which the diffusion barrier layer is substantially composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

59. (Unchanged) The method as defined in Claim 57, wherein the material from which the seed layer is substantially composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

60. (Unchanged) The method as defined in Claim 57, wherein the material from which the electrically conductive layer is substantially composed is selected from the group consisting of aluminum and copper.

61. (Once Amended) The method as defined in Claim 57, wherein the applying energy to the electrically conductive layer is performed with a furnace.

62. (Twice Amended) A method for manufacturing an interconnect structure, the method comprising:

providing a monocrystalline silicon layer of a semiconductor substrate assembly, said monocrystalline silicon layer defining a plane;

forming a dielectric material on the monocrystalline silicon layer;

forming a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said contact hole being oriented perpendicular to the plane of said monocrystalline silicon layer, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending parallel to the plane of said monocrystalline silicon layer;

forming a diffusion barrier layer on the trench and the contact hole, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

forming a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer within the trench and the contact hole and extending to terminate at the planar surface of the dielectric material, the material from which the diffusion barrier layer is composed having a melting point greater than that of the material from which the electrically conductive layer is composed, the

material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed, the material from which the electrically conductive layer is composed being selected from the group consisting of aluminum and copper; and

applying, omnidirectionally, energy to the electrically conductive layer to cause the electrically conductive layer to flow within the recess.

63. (Once Amended) The method as recited in Claim 62, wherein the applying energy to the electrically conductive layer is performed with a furnace.